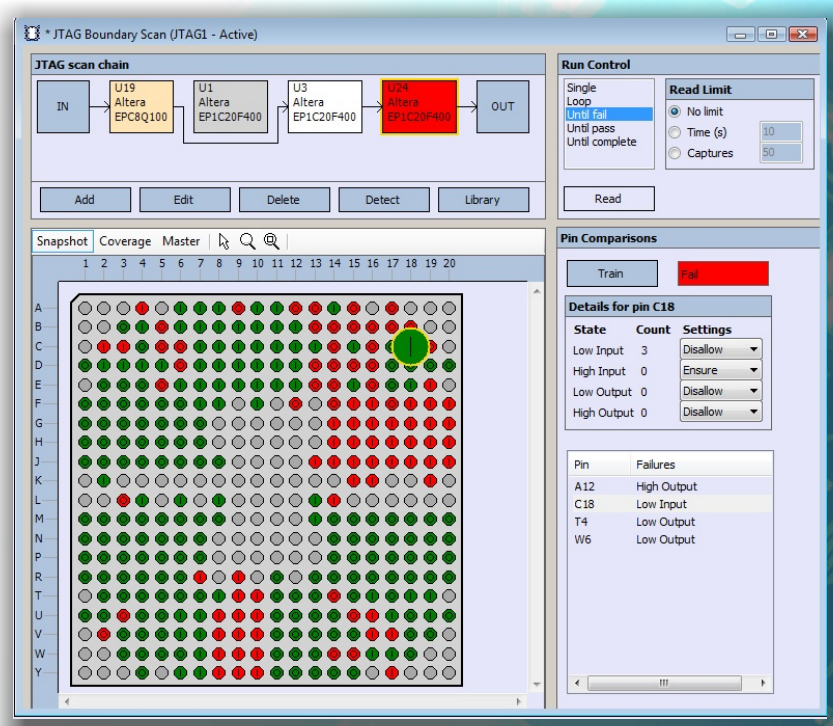
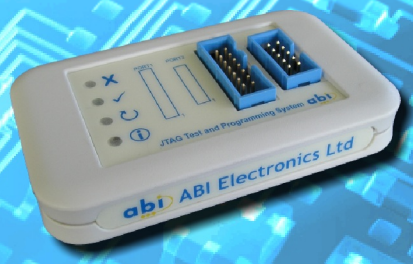
INCREASE YOUR TEST COVERAGE WITH JTAGMaster !





Improve Field Support •
Reduce Time to Market •
Increase Production Yield •
Improve Quality Assurance •
Lower Manufacturing Costs •
Decrease Debug Time Scales •
Reduce Investment Expenditure •

JTAGMaster

Boundary Scan Tester and In-System Programmer

The ABI JTAGMaster is a complete and powerful solution for the testing, fault-finding and programming of complex PCB assemblies with JTAG devices. Driven by the versatile AIM software, the JTAGMaster can also be integrated into existing setups.

With direct applications in sectors including Research & Development, Manufacturing and Test & Repair, the JTAGMaster is an invaluable tool giving you increased confidence in your hardware.

www.abielectronics.co.uk

What is the JTAGMaster?

With older technologies, in-circuit testing is carried out by accessing the pins of a device directly, usually using test clips. But with recent developments in electronics, most PCB assemblies are highly populated and do not allow access to the pins of a device, as is the case in BGA packages for instance.

The JTAGMaster gives you access to these devices that are bound to a JTAG chain with the purpose of carrying out testing, fault-finding and even programming operations. Boundary scan (or JTAG) is a widely recognised protocol implemented in most modern Programmable Logic Devices (eg CPLDs, FPGAs) and requires minimal hardware interface.

Where is JTAGMaster?

Field Service Engineering ✓
Production Engineering ✓
Design Engineering ✓
End of Line Testing ✓
Test Engineering ✓

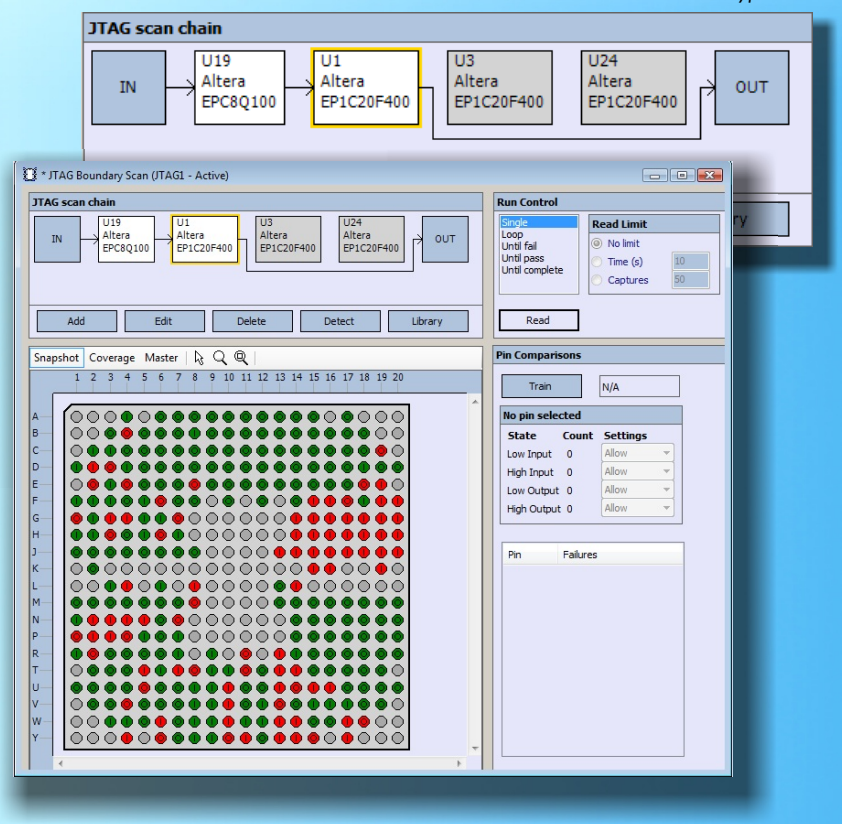
JTAGMaster - Quick and easy boundary scan testing

The JTAGMaster is aimed at the diagnosis and debugging of complex PCB assemblies containing single or multiple embedded devices.
Using the boundary scan test protocol, pins of each device can be individually and safely monitored to determine their functionality. This operation can be carried out on static or active boards over a pre-defined period of time.

Information from a board can be stored and recalled by any user for simple verification of the device(s) on a chain (with pass/fail results) or deeper investigation using the graphical viewer and zoom features. Analysing this information can lead to the detection of :

- Manufacturing defects
  (eg. open circuit/shorted pins)
- Logic errors
  (eg. pin failing to toggle/ faulty device)
- Programme errors
  (eg. incorrect/corrupted program)
- Faults in external circuitry
  (eg. missing or stuck input signal)

Devices in the chain can be bypassed



Automatic Functionality

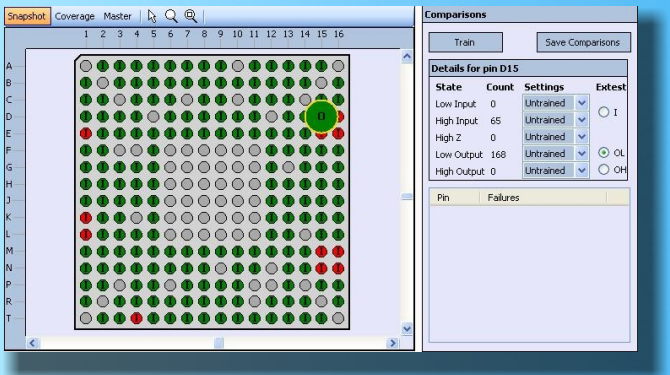
Various automatic functions and access levels are available with JTAGMaster :

- Automatic Chain Detection reduces the time consuming process of identifying devices.
- Automatic Training lets the software learn the status of the board by itself although manual intervention is also possible.
- Automatic Data Comparison for quick evaluation with pass or fail results.
- TestFlow Manager for easy to follow test sequences with data capture and report facility.

EXTEST Mode

This mode of testing, supported by the JTAGMaster, allows users to gain control of the pins of devices on the chain. The state of individual pins can be changed between output high or low and the resulting effect can be traced and monitored on other pins.

The effect of changing pin states may be checked on the same device or on other devices on the chain. It may also be traced on components outside of the chain, using an instrument such as the CircuitMaster 4000M for instance.

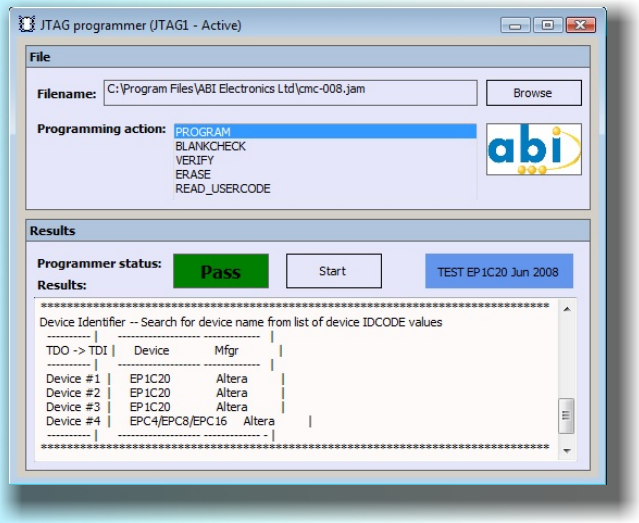


BGA device in EXTEST mode with pin E15 set as Output Low.

JTAGMaster - versatile programmer

In-system programming (ISP) is provided with the JTAGMaster which uses the JTAG interface to send programming and testing instructions to the device on the board. The JTAGMaster supports all the devices released by Altera, Xilinx, Lattice, Cypress, Atmel and all other manufacturers of devices that can be configured in-system using boundary scan (JTAG).

The JTAGMaster supports the file formats used as industry standards by PLD suppliers such as **SVF** (Serial Vector Format) and **JAM STAPL** (Standard Test and Programming Language).



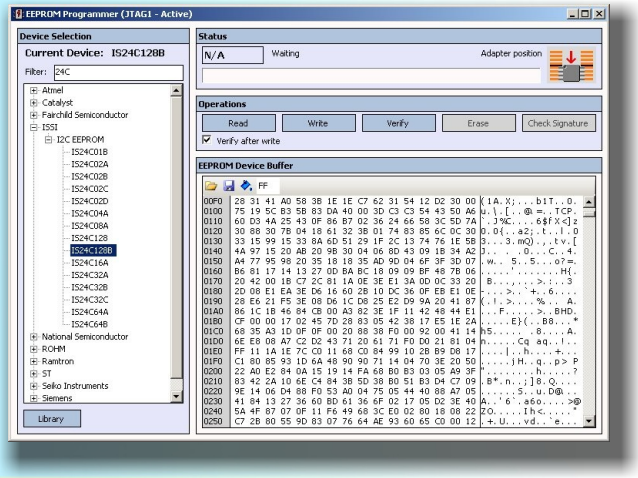
Integration with your existing system

The programming capabilities of the JTAGMaster can be easily transferred to an existing setup for seamless and central operation. Individual programming applications can be called up using a standard command line tool.

SPI, I²C and Microwire programming

The JTAGMaster unit is also capable of programming EEPROM devices using external adapters. Standard binary files are supported and can also be modified in the device buffer window. A wide range of EEPROM devices are present in the library which can be easily updated by users.
The signals and power connections are automatically mapped by the software depending on the protocol used:

- Serial Peripheral Interface (SPI)
- Inter-Integrated Circuit (I²C)
- Microwire (μWire)

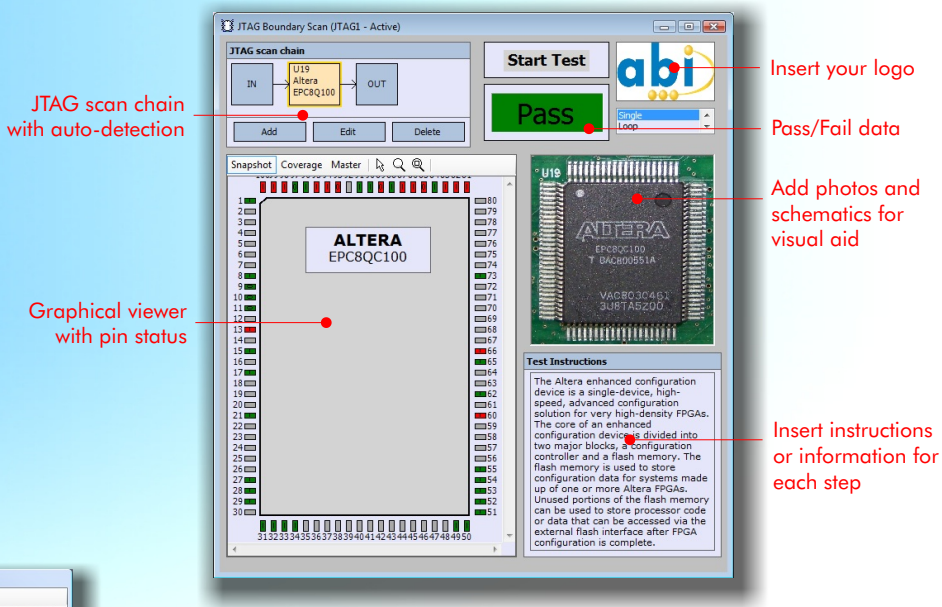


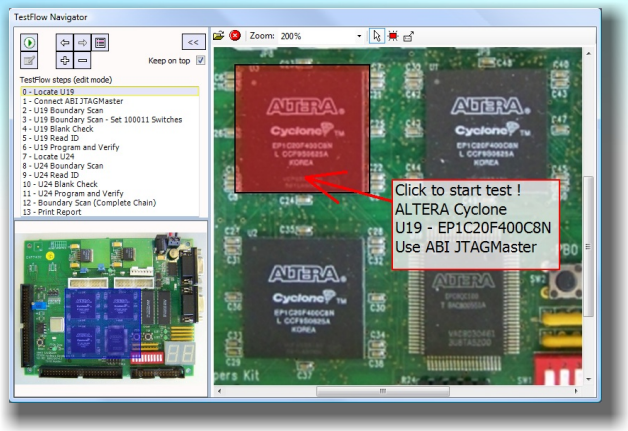
ABI Interface Manager Software (AIMs)

AIMs is a powerful and flexible platform designed for the control and operation of ABI products, including the JTAGMaster.

Customise this software yourself !

Application windows can be redesigned to suit particular needs and levels of operators. Layouts can be rearranged and instructions, photos or schematics can be added. Access levels can be easily managed through usernames and passwords. The internal library can be updated through BSDL files available from manufacturers' websites. AIMs also gives you the option to design custom packages for a better representation of your ICs in the graphical viewer.





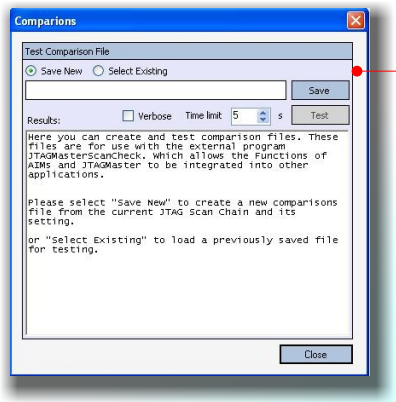
What is TestFlow?

A core feature of the software, the TestFlow Manager allows users to create automated test sequences in a simple, step by step structure. Each step may be customised with photos, schematics or instructions and can be set up to carry out tasks as simple or as complex as required.

Each step of the TestFlow retains the information, the settings and the master data for direct comparison. At any point during a TestFlow run, users can enter their own comments which will be included in a test report.

JTAGMaster Scan Check (Optional)

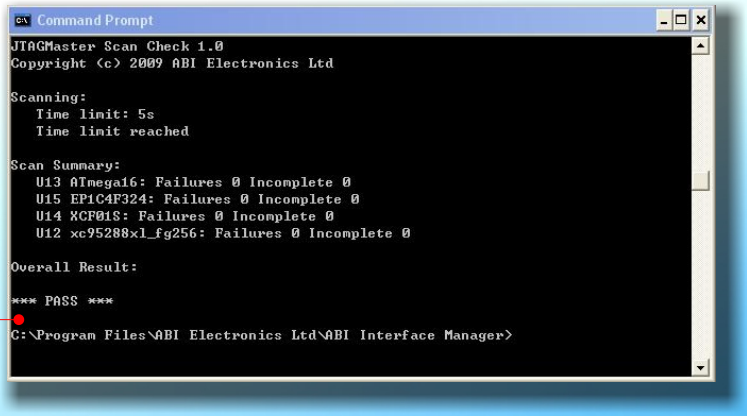
The JTAGMaster Scan Check option is an application which runs separately from the AIMs software. It can be used as a standalone alternative to run boundary scan tests.
The AIMs software is used as a "master" to acquire checked and approved data from a chain whilst Scan Check can be used on other stations to simply run the tests and return a pass or fail result.



Use the AIMs software to save master data from the chain

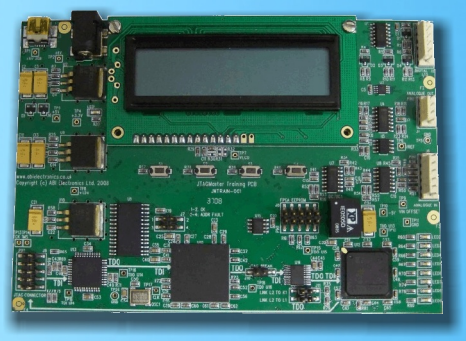
and

run Scan Check at another station to verify the chain



Comprehensive Training Package

Make the most of your JTAGMaster with the training package available from ABI Electronics. The training exercises, controlled by a TestFlow in the AIMs software, cover the basics of JTAG, the programming section and the boundary scan capabilities.
Ideal for users new to JTAG or to give in-house product training.



Technical Specifications

Electrical Requirements

Operating voltage: 5V (powered by USB port)
Power consumption: 500mW
CE approved & RoHS compliant

Physical Specifications

Dimensions: 83 x 52 x 16mm
Weight: 200g

Environmental Requirements

Operating temperature: 0°C to 50°C
Storage temperature: 0°C to 70°C
Humidity: up to 80% non-condensing

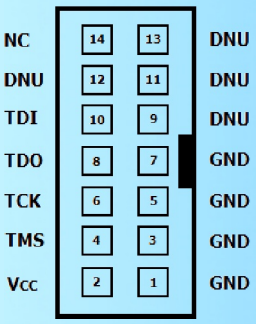
Comprehensive Training Package (Optional) Computer Requirements

Microsoft Windows XP™ or Vista™
Pentium 4 or above
Minimum RAM: 512 MB
Hard disk space: 200 MB
USB interface port (x2)
Mouse, keyboard & monitor

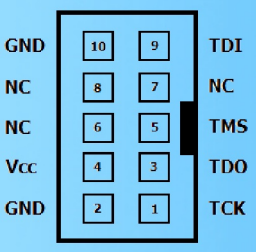
Included Accessories

10-pin ISP interface cable assembly
14-pin configurable ISP interface cable assembly
USB cable
Software CD (with drivers and user manual)
Activation dongle (USB)

PORT 1 Xilinx Pinout



PORT 2 Altera Pinout



TDI - Data to device
TDO - Data from device
TCK - Clock signal
TMS - JTAG stage machine control
Vcc - Target power supply
NC - No connected
DNU - Do not use

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